REMARK

Applicant respectfully requests reconsideration of this application as amended and in view of the following remark. Claims 1, 2, 15, 16, 21, 25 & 28 have been amended. No claims have been canceled and new claims 29 & 30 have been added. Therefore, claims 1-30 are presented for examination.

35 U.S.C. §112 Rejections

The Examiner rejected claims 1-28 under 35 U.S.C. 112, first paragraph as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the Examiner objected to the use of the term "native bus transaction" as new matter, because the term was never discussed in the original specification.

Although the applicant agrees that the specific term "native bus transaction" was never used in the original specification, he respectfully asserts that there is support for the elements represented and conveyed by the term in the specification and the term is, therefore, not new matter. However, in the interests of clarity and to eliminate any confusion that may have resulted due to the use of the term, the applicant has modified the claims to remove the adjective "native" from the term "native bus instruction."

A brief discussion of predefined bus stimuli instructions as disclosed in the specification is in order to help clarify the scope of the claimed invention for the Examiner.

As discussed in the background, the prior art methods of validating and testing bus/component interactions generally include the use of a processor to generate and drive the specific bus transactions of interest. In this type of testing system, the processor is typically instructed in assembly language about the bus transactions the processor is to generate. Unfortunately, it may not be possible to precisely control all of the factors relating to the test sequence of bus transactions using assembly language instructions. See Page 7, line 13 – Page 8, line 9.

For example, a processor might be directed in assembly language to move the data in a memory register to a graphics controller register over a bus. The processor would then translate the assembly instructions into a bus transaction request particular to the type of bus over which the transaction would be transmitted (i.e. the specific bus transaction generated for performing the data move would depend on the specific bus over which the bus transaction is to be sent). The assembly language move command is in a sense generic.

The assembly language move instruction of the example does not provide mechanisms for controlling the particular manner in which the signal corresponding to the bus transaction is generated and transmitted. For instance, a user testing the graphics controller, memory, and bus combination of the example might want to induce a delay between an address phase and a data phase of the bus transaction to test whether such a delay would cause an error. However, the timing between bus transactions phases is outside the scope of resolution of the "generic" assembly move command.

The claims in the application are directed to a method and apparatus that give control over the particular factors related to the bus transaction on a bus. Typically, the

predefined bus stimuli instruction would be in the form of a lower level language more suited to the particular aspects of a bus transaction on a particular bus. For example, the predefined bus stimuli instruction for the data move in the previous example might have a command to delay the data phase by a particular number of clock cycles after the address phase.

To contrast assembly language instructions with predefined bus stimuli instructions: a predefined bus stimuli instruction represents signals, the transmission thereof, and other elements (collectively "bus stimuli") that are associated with a bus transaction on a particular bus (i.e. the instructions are "predefined" for the particular bus); whereas, the assembly language instruction is translated into signals corresponding to a bus transaction depending on the particular bus over which the bus transaction is to be transmitted, but the assembly language instruction does not provide for the specific manner in which the signals corresponding to the bus transaction are configured or transmitted. See Detailed Description in general for further discussion with regard to "bus stimuli" and "predefined bus stimuli".

The adjective "native" was used to denote that the predefined bus stimuli instructions represent the bus transaction as it is configured with respect to a particular bus (i.e. a bus transaction that is "native" to a particular bus) rather than an instruction, such as one that may be issued in assembly language, that is generic relative to the particular bus.

35 U.S.C. §102 Rejections,

Gates (5,701,409)

The Examiner has rejected claims 1, 2, 4-6 & 9-28 under 35 U.S.C. §102(e) as being anticipated by Gates. The Applicant respectfully disagrees with the Examiner's rejection and asserts the Examiner has failed to established a prima facie case of anticipation, because Gates fails to teach all the recited claim limitations in the claims. In order for a reference to be anticipatory, it must teach each and every aspect of the claimed invention.

The Examiner also rejected claims 3,7 & 8 under 35 U.S.C. §103(a) as being unpatentable over Gates in view of Official Notice taken with regard to elements in the claims and motivations to combine the elements of Official Notice with those recited in Gates. The applicant respectfully asserts that the Examiner has not made a prima facie case of obviousness as Gates in combination with the Official Notices fails to teach, suggest or motivate all of the limitations of the claims.

Claim 1

Claim 1 was rejected as being anticipated by Gates. The applicant respectfully asserts that Gates does not teach all of the elements of claim 1.

As understood by the applicant, Gates teaches an integrated circuit that generates an error on a bus from an error command that is loaded into the circuit. See Abstract ("During test, an error command is loaded into a command register of the bus generation circuit"). The purpose of generating an error using the circuit of the Gates reference is to test how a bus responds and corrects the error. See Col. 5, lines 26-30.

In contrast, claim 1 recites a system with "at least one phase generator to provide signals to the bus corresponding to the bus transaction". Although, the bus transaction transmitted over the test bus by the claim 1 system in certain circumstances may cause an error condition on the bus, it is not the necessary result of driving a bus transaction; whereas, the entire purpose of the Gates circuit is to cause an error condition on the test bus by driving an error signal responsive to a given error command. In short, the Gates circuit does not generate and transmit onto the bus "signals ... corresponding to [a] bus transaction" as represented by "predefined bus stimuli instructions"; rather, it generates an error condition over the bus responsive to an error command.

Furthermore, the Gates reference does not teach the claim 1 element of "at least one instruction memory to store a predefined bus stimuli instruction". See discussion supra with regard to "predefined bus stimuli". Gates teaches a memory that stores an error command. As understood by the applicant, an error generation command is not the same as a "predefined bus stimuli instruction". The "predefined bus stimuli instruction" represents a bus transaction, and the error command does not.

For at least these reasons, claim 1 is allowable over the Gates reference.

Dependent Claims 2-14

Claims 2-14 are dependent on claim 1 and accordingly, they are allowable over Gates for at least the same reasons as provided for claim 1 supra.

Claim 15

For at least the same reasons as given for claim 1, Gates does not teach "an instruction memory storing digital data representing a predefined sequence of bus stimuli". In addition, the relied upon sections of the reference do not disclose or teach; a flow logic device responsive to the instruction memory, a request logic device responsive to the instruction memory, a data logic device responsive to the instruction memory, a data memory coupled to the data logic device storing data to be exchanged with agents on the bus, a system protocol generator coupled to the bus and the flow logic device, an arbitration protocol generator coupled to the flow logic device and the bus, a request protocol generator coupled to the flow logic device, the request logic device and the bus, a snoop/error protocol generator coupled to the request logic device and the bus, and a data protocol engine coupled to the data logic device.

For at least these reasons, claim15 is allowable over the Gates reference.

Claim 16

For at least the same reasons as given for claim 1, Gates does not teach a "means for storing instructions representing predefined bus stimuli", nor does it teach "means for providing signals to the bus in response to the stored information". Accordingly, claim 16 is in a condition for allowance over the Gates reference.

Dependent Claims 17-20

Claims 17-20 are dependent on claim 16 and accordingly, they are allowable over Gates for at least the same reasons as provided for claim 16 supra.

Claim 21

For at least the same reasons as given for claim 1, Gates does not teach a "receiving instruction words representing predefined bus stimuli", nor does it teach "converting the instruction words to signals that, when applied to the bus, execute at least one phase of a bus transaction". Accordingly, claim 21 is in a condition for allowance over the Gates reference.

Dependent Claims 22-24

Claims 22-24 are dependent on claim 21 and accordingly, they are allowable over Gates for at least the same reasons as provided for claim 21 supra.

Claim 25

For at least the same reasons as given for claim 1, Gates does not teach a "defining the sequence of [native] bus transactions", and "assembling the sequence of bus transactions into an object file representing bus stimuli", nor does it teach "executing the bus stimuli". Accordingly, claim 21 is in a condition for allowance over the Gates reference.

Dependent Claims 26-28

Claims 26-28 are dependent on claim 25 and accordingly, they are allowable over Gates for at least the same reasons as provided for claim 25 supra.

New Claims 29 & 30

New claims 29 & 30 are allowable for at least the same reasons as given for claim 1 supra.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, the Applicant respectfully requests the Examiner to withdraw the remaining rejections and to immediately issue a Notice of Allowability.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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